

# Very low capacitance unidirectional ESD protection diode array

18 September 2024

Product data sheet

# 1. General description

Extremely low capacitance unidirectional ElectroStatic Discharge (ESD) protection diode array, part of the TrEOS protection family. This device is housed in a DFN2510-10 (SOT1165-3) leadless ultra small Surface-Mounted Device (SMD) plastic package, designed to protect four signal lines from the damage caused by ESD and other transients.

### 2. Features and benefits

- Unidirectional ESD protection for four signal lines
- V<sub>RWM</sub> = 3.3 V device
- Extremely low clamping voltage to protect sensitive I/Os
- IEC 61000-4-5 (surge): I<sub>PP</sub> = 7.9 A peak pulse (average measured)
- Extremely low diode capacitance C<sub>d</sub> = 0.29 pF typical at 1.5 V
- ESD protection up to ±15 kV according to IEC 61000-4-2
- Leadless ultra small DFN2510-10 (SOT1165-3) surface mount package

# 3. Applications

- Cellular handsets and accessories
- Portable electronics
- Communication systems
- · Computers and peripherals
- USB3.2 data lines

### 4. Quick reference data

#### Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>RWM</sub>	reverse standoff voltage		-	-	3.3	V
C <sub>d</sub>	diode capacitance	f = 1 MHz; V <sub>R</sub> = 1.5 V; T <sub>amb</sub> = 25 °C	-	0.29	0.34	pF



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# 5. Pinning information

**Table 2. Pinning information** 

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CH1	channel 1 ESD protection		СН1 СН3
2	CH2	channel 2 ESD protection	1 10	CH2   CH4 
3	GND	ground		本本本
4	CH3	channel 3 ESD protection		GND
5	CH4	channel 4 ESD protection		<b>←</b>
6	n.c.	not connected		
7	n.c.	not connected		<u> </u>
8	GND	ground		本。个人
9	n.c.	not connected	5 6	
10	n.c.	not connected	Transparent top view	<u> </u>
			DFN2510-10 (SOT1165-3)	aaa-016329

# 6. Ordering information

**Table 3. Ordering information** 

Type number Package				
	Name	Description	Version	
PUSB3FC4		plastic, leadless extremely thin small outline package; 10 terminals; 0.5 mm pitch; 2.5 mm x 1 mm x 0.5 mm body	SOT1165-3	

# 7. Marking

Table 4. Marking codes

Type number	Marking code
PUSB3FC4	A2A

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# 8. Limiting values

#### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{RWM}$	reverse standoff voltage			-	3.3	V
I <sub>PPM</sub>	rated peak pulse current	t <sub>p</sub> = 8/20 μs	[1]	-7	7	Α
T <sub>stg</sub>	storage temperature			-65	150	°C
T <sub>amb</sub>	ambient temperature			-40	125	°C
ESD maximun	n ratings				•	·
V <sub>ESD</sub>	valta aa	IEC 61000-4-2; contact discharge	[2]	-15	15	kV
		IEC 61000-4-2; air discharge	[2]	-15	15	kV

- [1] Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC 61000-4-5.
- [2] Device stressed with ten non-repetitive ESD pulses.

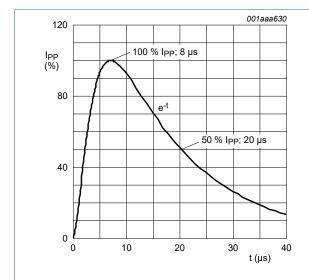


Fig. 1.  $8/20~\mu s$  pulse waveform according to IEC 61000-4-5

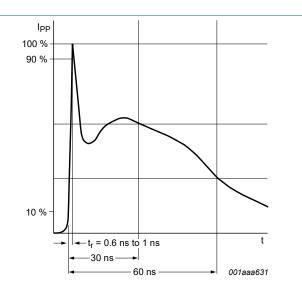


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

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# 9. Characteristics

**Table 6. Characteristics** 

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{BR}$	breakdown voltage	I <sub>R</sub> = 1 mA; T <sub>amb</sub> = 25 °C		5.5	9	-	V
$V_{CL}$	clamping voltage	I <sub>TLP</sub> = 8 A; t <sub>p</sub> = 100 ns; T <sub>amb</sub> = 25 °C	[1]	-	3.5	-	V
		I <sub>TLP</sub> = 16 A; t <sub>p</sub> = 100 ns; T <sub>amb</sub> = 25 °C	[1]	-	5.5	-	V
		I <sub>PPM</sub> = 7 A; t <sub>p</sub> = 8/20 μs; T <sub>amb</sub> = 25 °C	[2]	-	3.5	-	V
I <sub>RM</sub>	reverse leakage current	V <sub>RWM</sub> = 3.3 V; T <sub>amb</sub> = 25 °C		-	1	100	nA
R <sub>dyn</sub>	dynamic resistance	I <sub>R</sub> = 10 A; t <sub>p</sub> = 100 ns; T <sub>amb</sub> = 25 °C	[1]	-	0.26	-	Ω
		I <sub>R</sub> = -10 A; t <sub>p</sub> = 100 ns; T <sub>amb</sub> = 25 °C	[1]	-	0.26	-	Ω
$C_d$	diode capacitance	f = 1 MHz; V <sub>R</sub> = 1.5 V; T <sub>amb</sub> = 25 °C		-	0.29	0.34	pF

- [1] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008 on pin 2
- [2] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.

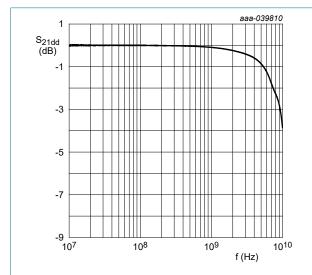


Fig. 3. Differential mode insertion loss; typical values

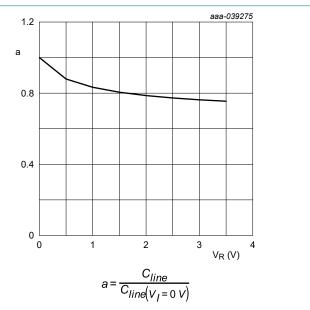
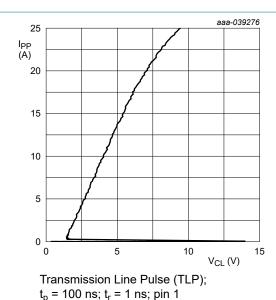
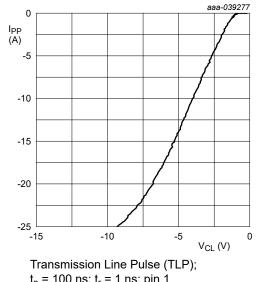


Fig. 4. Relative capacitance as a function of reverse standoff voltage; typical values

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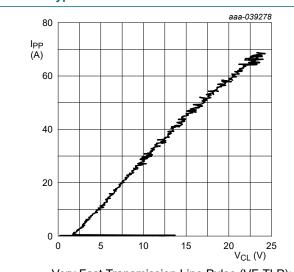


Dynamic resistance with positive clamping; Fig. 5. typical values



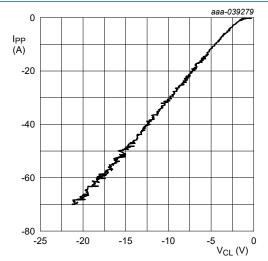
 $t_p = 100 \text{ ns}; t_r = 1 \text{ ns}; \text{pin } 1$ 

Dynamic resistance with negative clamping; Fig. 6. typical values



Very Fast Transmission Line Pulse (VF-TLP);  $t_p = 5 \text{ ns}; t_r = 600 \text{ ps}; \text{pin } 1$ 

Dynamic resistance with positive clamping; Fig. 7. typical values



Very Fast Transmission Line Pulse (VF-TLP);  $t_p = 5 \text{ ns}; t_r = 600 \text{ ps}; \text{pin } 1$ 

Dynamic resistance with negative clamping; Fig. 8. typical values

# Very low capacitance unidirectional ESD protection diode array

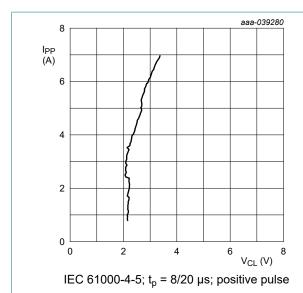


Fig. 9. Dynamic resistance with positive clamping; typical values

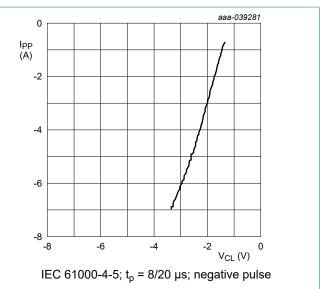


Fig. 10. Dynamic resistance with negative clamping; typical values

### Very low capacitance unidirectional ESD protection diode array

# 10. Application information

The device is designed for the protection of four unidirectional data or signal lines from surge pulses and ESD damage.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

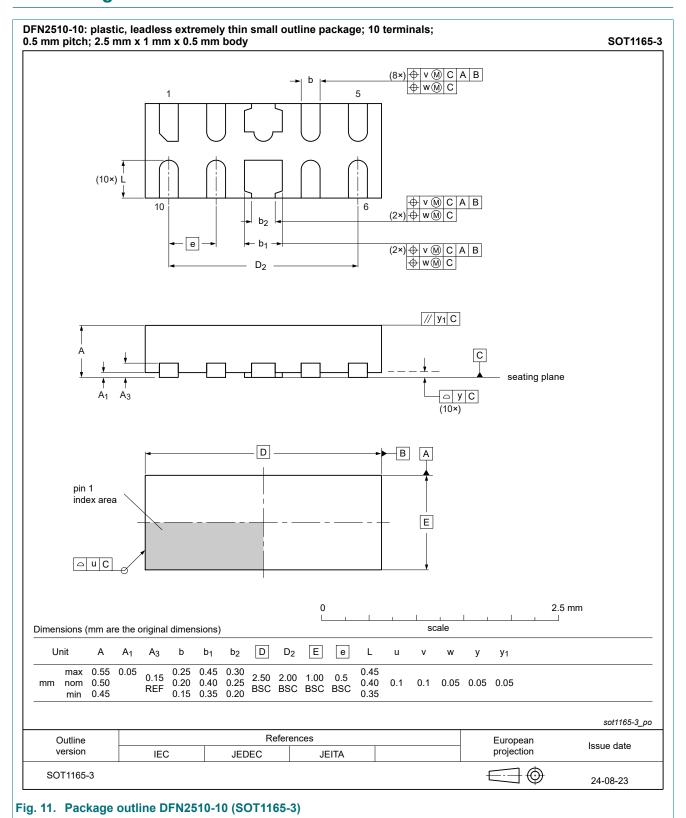
#### Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

- 1. Place the device as close to the input terminal or connector as possible.
- 2. Minimize the path length between the device and the protected line.
- 3. Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductors.
- 5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- 6. Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

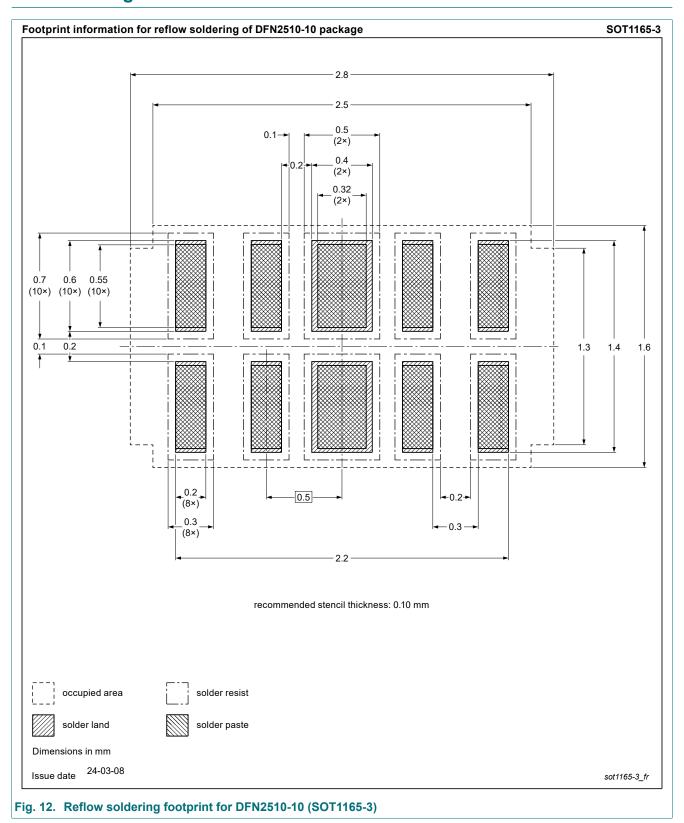
### Very low capacitance unidirectional ESD protection diode array

# 11. Package outline



Very low capacitance unidirectional ESD protection diode array

# 12. Soldering



# Very low capacitance unidirectional ESD protection diode array

# 13. Revision history

### **Table 7. Revision history**

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Data sheet ID	Release date	Data sheet status	Change notice	Supersedes			
PUSB3FC4 v.4	20240918	Product data sheet	-	PUSB3FC4 v.3			
Modifications:	Chapter "Package or	utline": Typo correction fo	r w, y, y <sub>1</sub>				
PUSB3FC4 v.3	20240523	Product data sheet	-	PUSB3FC4 v.2			
PUSB3FC4 v.2	20240517	Objective data sheet	-	PUSB3FC4 v.1			
PUSB3FC4 v.1	20240320	Objective data sheet	-	-			

#### Very low capacitance unidirectional ESD protection diode array

# 14. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
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